Uplink Interference Cancellation in HSPA: Principles and Practice

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Abstract

This paper provides the principles and practice of how interference cancellation (IC) can be implemented for the uplink in a 3GPP HSPA NodeB (Base Station) receiver. Uplink interference cancellation is a capacity enhancing technique that can be added to a NodeB receiver without the need to modify user equipment (UE), 3GPP specifications or network coverage. Details are provided on the algorithm, implementation and the corresponding system performance.

Introduction

The uplink of WCDMA was significantly enhanced in 3GPP Release 6 with the introduction of the enhanced uplink feature also referred to as HSUPA (High Speed Uplink Packet Access). In particular, the feature introduced the capability to schedule packet data transmissions on the uplink in a spectrally efficient manner. The key attribute of the enhanced uplink feature was the Hybrid automatic repeat request (H-ARQ) method that introduces time diversity in fading channel environments which in turn improves spectral efficiency as well as facilitates delay critical applications by targeting early packet terminations. The introduction of a 2ms transmission time interval (TTI) allows for a very short latency in the uplink packet data transmission. Furthermore, a centralized uplink scheduler at the NodeB (base station) facilitates proportional fair scheduling of packet data amongst all the users. In 3GPP Release 7, the discontinuous transmission (DTX) feature as part of the Continuous Packet Connectivity work item was introduced on the uplink with a key emphasis on improving the uplink capacity and user experience of real-time applications such as VoIP. In addition, the 16-QAM feature boosted the peak rate from 5.76 Mbps to 11.52 Mbps. In 3GPP Release 8, a few more enhancements were further introduced. The random access channel performance was enhanced significantly via the Enhanced Uplink in CELL_FACH feature, which allowed for fast power control and H-ARQ transmission on the uplink in CELL_FACH state. Further the MAC segmentation feature introduced as part of the Improved Layer 2 for Uplink work item further improves link budget issues associated with 2ms TTI operation, by allowing for Radio Link Control (RLC) PDUs to be further segmented dynamically in accordance with the available UE power headroom. In this paper, we present the principles and practice of further enhancing the uplink capacity of HSPA by introducing uplink IC to the

NodeB receiver. This feature requires no change to the air interface, which implies no impact to the UE.

The WCDMA uplink is a multiple access channel. A conventional single user matched filter receiver is strictly suboptimal in terms of capacity. Receivers with advanced IC algorithms can significantly improve the system performance. With uplink IC, cellular networks can operate at higher interference level since the effective interference is reduced after IC. For voice communication, this will directly translate to increased number of voice users. For data services, strong interference from high data rate users can be removed to improve the reception of low data rate users. Combined with opportunistic scheduling, interference cancellation yields higher data throughput and improved fairness among users.

The notion of IC covers a broad research area of the seminal multi-user detection (MUD) theory [2]. We consider non-linear IC techniques that reconstruct and subtract successfully decoded signals from the receiver sample buffer. This notion of IC is well known and was proposed for CDMA many years ago [4]; however, implementation complexity was quite challenging. With current state of the art technology, IC is no longer merely a topic of academic research. CDMA IC is now commercially viable. For example, the QUALCOMM CSM6850 chipset solution for the EV-DO RevA/B reverse link offers both pilot and traffic IC.

This paper is organized as follows. We first describe the motivation of uplink IC. We then describe a few forms of successive interference cancellation followed by a description of the fundamental processing blocks required for post decoding IC. Next, we describe the practical aspects of uplink IC in an HSPA NodeB receiver. Finally both link and system performance benefits of uplink IC are presented.

Motivation of Uplink Interference Cancellation

The WCDMA uplink channel is, by nature, an interference-constrained multiple-access channel. All active users simultaneously transmit asynchronously over the same bandwidth, and each user's signal is interfering with other users' signal. The interference, at the NodeB receiver antenna input is composed of three components namely, intra-cell interference, inter-cell interference and thermal noise.

The intra-cell interference component represents the sum of the WCDMA uplink waveforms of all the users who communicate with the NodeB cell. This also includes the self interference caused by the multi-path channel on each user's transmitted waveform. In general these waveforms are non-orthogonal to each other due to the fact that the users' transmissions are offset with respect to each other and the fact that a non-zero cross-correlation exists between each user's scrambling code. Hence, the process of de-scrambling and de-spreading a particular user's waveform with its own scrambling code and channelization code respectively (also referred to as a matched filter) is not enough to fully eliminate the other users' energy or the self interference caused due to the multi-path channel.

The inter-cell interference component represents the sum of the WCDMA waveforms of all the users who do not communicate with the NodeB cell under consideration. The Node-B is not aware of these users and hence does not power control or rate control these users

Such interference among users fundamentally limits the maximal data throughput of an uplink cellular system, as well as the maximal number of co-existing users. Assume that we have a total of *K* active users transmitting to the same receiver in an isolated cell environment, and the signal from the i^{th} user arrives at the receiver with power P_i. If we further assume the channel is an additive while Gaussian noise (AWGN) channel with noise spectral density N_0, then the signal-to-noise ratio at the output of the i^{th} user's matched filter is $\frac{P_i}{N_0 W + \sum_{k \neq i} P_k}$. According to classical Shannon theory [3], the transmission rate of the i^{th} user, in bits/s/Hz, is upper bounded as follows:

$$R_i \leq \log_2\left(1 + \frac{P_i}{N_0 W + \sum_{k \neq i} P_k}\right).$$

Notice that in a classical power controlled CDMA uplink, a specific user's power is generally much lower than noise power, which includes both thermal noise $N_0 W$ and the other user interference $\sum_{k \neq i} P_k$. Therefore, using first order Taylor expansion, the sum of transmission rates that each individual user could achieve (or equivalently, cell throughput) will not exceed

$$R_{total} = \sum_i R_i \leq \sum_i \log_2\left(1 + \frac{P_i}{N_0 W + \sum_{k \neq i} P_k}\right) \approx \frac{1}{\ln 2} \cdot \sum_{i=1}^{K} \frac{P_i}{N_0 W + \sum_{k \neq i} P_k}$$

For a sufficiently large *K*, the bound above leads to a spectral efficiency of $(\ln 2)^{-1}$ bits/s/Hz. On the other hand, however, the sum-rate capacity of a Gaussian multiple-access channel is [3]

$$C = \log_2\left(1 + \frac{\sum P_i}{N_0 W}\right),$$

which can be much larger than $(\ln 2)^{-1}$ bits/s/Hz, if the total power of all users is sufficiently large. For example, if the total signal power is 10 times the noise power, then the theoretical achievable throughput would be $\log_2(11) = 3.46$ bits/s/Hz, which is much larger than sum of the maximal rate that each individual user could transmit, assuming a single user matched filter receiver is adopted and all the other users' signals occur as interference. Obviously, a single user matched filter receiver is not the optimal scheme in a multiple-access scenario.

The surprising fact about this capacity of a multiple-access channel is that the sum rate can be as large as the rate that a single transmitter can achieve given the total power of all users. Therefore, a critical measure that determines uplink system performance is Noise Rise (NR), defined as

$$NR = 1 + \frac{\sum P_i}{N_0 W}.$$

Theoretically, the ideal capacity of a multiple-access channel can be achieved through an "onion peeling" process, where users are decoded in a successive manner, and the signal of successfully decoded users are subtracted from the waveform before decoding the next user. Therefore, a "cleaner" signal is available for the users yet to be decoded. Such procedure is typically referred to as successive interference cancellation (SIC).

The multiple-access channel capacity is achieved under the assumption that the decoded signal is fully removed from the received waveform. In practical implementations, however, cancellation is not ideal and there will be residual interference remaining. Exactly how much interference could be removed depends on many factors, such as channel estimation quality, data decision quality, etc. To further quantify the amount of interference cancelled, we need to introduce an important measure namely the interference cancellation efficiency β.

Let y denote the noiseless signal that we want to reconstruct, and $\hat{y}$ denote the corresponding reconstructed signal. We define the interference cancellation efficiency as

$$\beta = 1 - \frac{|y - \hat{y}|^2}{|y|^2}$$

where $\beta \le 1$.

Notice that β indicates the quality of signal reconstruction. β =1 represents perfect cancellation where y is precisely reconstructed. A small positive β represents a signal that is not fully reconstructed and there is residual interference after cancellation.
A negative β represents that we have falsely reconstructed signal, and instead of removing interference, we have added more interference to the waveform.

In practice, signal reconstruction quality depends on both channel estimation and symbol decision quality. Without loss of generality, we simply assume that the channel has a single path and the transmitted symbols are BPSK-modulated. The cancellation efficiency can be further expanded as

$$\beta = 1 - E\left[\frac{\left|h_k \cdot d_k \cdot \underline{c}_k - \hat{h}_k \cdot \hat{d}_k \cdot \underline{c}_k\right|^2}{\left|h_k \cdot d_k \cdot \underline{c}_k\right|^2}\right] = 1 - E\left[\frac{\left|h_k \cdot d_k - \hat{h}_k \cdot \hat{d}_k\right|^2}{\left|h_k \cdot d_k\right|^2}\right]$$

$$= 1 - \underbrace{E\left[\left|d_k - \hat{d}_k\right|^2\right]}_{\substack{\text{Mean Square} \\ \text{Symbol Estimation Error}}} - E\left[\left|\hat{d}_k\right|^2\right] \cdot \underbrace{E\left[\frac{\left|h_k - \hat{h}_k\right|^2}{\left|h_k\right|^2}\right]}_{\substack{\text{Normalized Mean Square} \\ \text{Channel Estimation Error}}} - E\left[\frac{\mathrm{Re}\left(h_k^* \hat{d}_k \left(h_k - \hat{h}_k\right)\left(d_k^* - \hat{d}_k^*\right)\right)}{\left|h_k\right|^2}\right]$$

Here $d_k \in \{+1, -1\}$ is the transmitted symbol, and $\underline{c}_k$ is the spreading sequence corresponding to d_k. In the above equation, $\left(h_k - \hat{h}_k\right)$ represents the channel estimation error while $\left(d_k - \hat{d}_k\right)$ represents the data symbol estimation error. Notice that in general, the last term is zero under a practical assumption that the symbol estimation error is uncorrelated to the data symbol estimation error[1]. The equation indicates that cancellation efficiency is dependent on the mean squared error of symbol decisions, as well as on the normalized mean squared error of channel estimation. For post decoding IC, the symbol estimation is error free and the IC efficiency is then only impacted by the mean squared error of the channel estimation. It is then as expressed as follows:

$$\beta = 1 - E\left[\left|\hat{d}_k\right|^2\right] \cdot E\left[\frac{\left|h_k - \hat{h}_k\right|^2}{\left|h_k\right|^2}\right]$$

Interference cancellation can be applied not only for the purpose of data throughput improvement, but also to increase the number of co-existing users that have a constant bit rate traffic, say, voice users.

Assume an acceptable quality of service for voice traffic requires a signal-to-noise-ratio (SNR) of γ, and assume we have perfect power control such that each user's received power is controlled to a constant level P, we have

$$\frac{P}{N_0 W + (K-1)P} \geq \gamma .$$

The maximal number of voice users allowed in this system would be

$$K \leq \frac{1}{\gamma} - \frac{N_0 W}{P} + 1$$

[1] This assumption may not be precise for a multi-path scenario. It also ignores the fact that a symbol decision is dependent on the channel estimation quality. However, in the case of post decoding IC, such an assumption is unnecessary, since $d_k = \hat{d}_k$.

Suppose that after interference cancellation we can remove a fraction β of the total interference seen by a given user, where $0 < \beta < 1$, then the total number of voice users that can be supported in the cell can be derived as follows[2]:

$$\frac{P}{N_0 W + (1-\beta)(K-1)P} \geq \gamma$$

$$K \leq \frac{1}{\gamma(1-\beta)} - \frac{N_0 W}{P(1-\beta)} + 1.$$

Notice that in this case, the number of co-existing users highly depends on how much interference we could cancel. For example, if $\beta = 0.5$ in the above formula, then the number of users increases by a factor of 2.

It has been shown by Viterbi [4] that, through successive interference cancellation, the total bit rate of a practical frame synchronous CDMA system could approach within a factor of Shannon limit. The analysis was based on the assumption that users transmitted at the same rate with exponential power allocation, i.e., $P_k = P_1(1+P_1)^{k-1}$, where P_k is the power of the *k*-th user. It was also further demonstrated in [5] that this result could be extended to a frame asynchronous system where users do not necessarily transmit at the same bit rate and have exponential power profile. The effect of non-perfect cancellation on cell capacity was briefly discussed in [8].

[2] Notice that here we ignore the fact that in practical systems, some channels may not benefit from interference cancellation. For example, control and overhead channels have strict latency requirements that prevent them from being processed by the IC subsystems.

Principles of Uplink Interference Cancellation

Among various IC algorithms, we first consider successive IC (see Figure 1), a simple but powerful scheme proposed during the early development of CDMA [4]. Users are ordered by their chance of successful decoding and the packet of the strongest user is decoded first. After a packet is decoded, the signal is reconstructed and subtracted from the received signal. The rest of users are ordered again for next round of decoding. The procedure is performed iteratively over all users.

In general, a user decoded later benefits from cancellation of previous users and encounters improved Signal to Interference and Noise Ratio (SINR). However, a large delay is inevitable since users are decoded and cancelled successively.

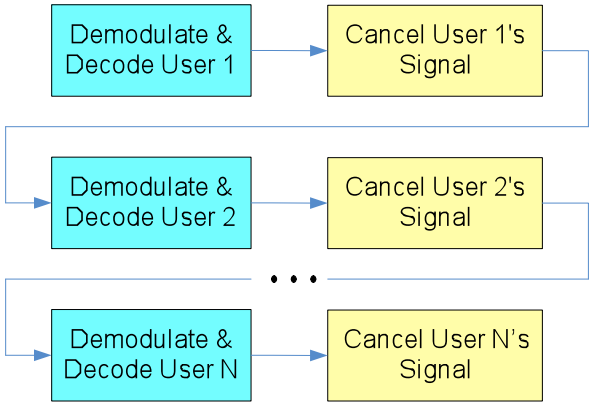

Figure 1: Successive Interference Cancellation

To address the delay issue in successive IC, we consider iterative parallel IC shown in Figure 2. This scheme is more attractive from implementation perspective. Multiple users are decoded and cancelled from the received signal simultaneously. If a user fails decoding in the first iteration, it will be decoded again in the subsequent iteration. The processing power is distributed among multiple parallel demodulators and decoders. Thus the tradeoff between delay and complexity is well balanced. Moreover, the performance of parallel IC can approach successive IC with a small number of iterations.

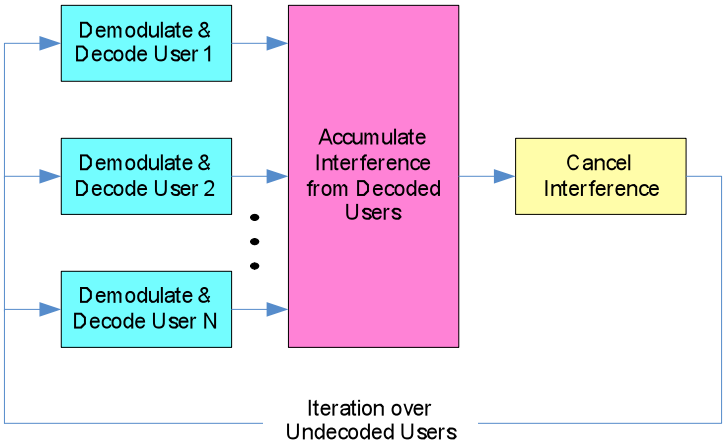

Figure 2: Iterative Parallel Interference Cancellation

Smart scheduling can be added to parallel IC to further improve performance. The Group IC scheme is illustrated in Figure 3. Users are divided into groups according to certain criterion and then Parallel IC is performed on high priority groups to low priority groups successively. Iterative processing can be applied to the users fail in the first IC iteration. Actually this scheme is a combination of Successive and Parallel IC in case users are grouped according to their decoding probabilities. The grouping approach can be also used to address the delay constraints, in which the low latency users are scheduled to high priority group.

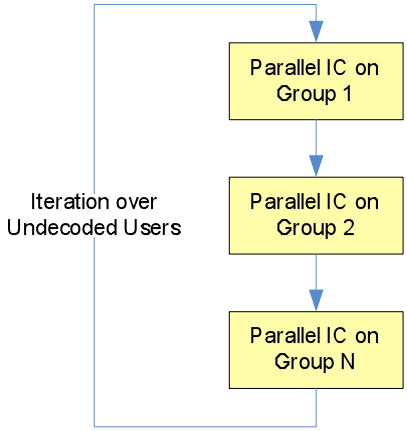

Figure 3: Iterative Group Interference Cancellation

Note that in any of the above schemes, even if a user fails to decode, one could attempt to cancel a portion of the user's waveform by performing soft interference cancellation. In this case, minimum mean square error (MMSE) estimates of the data symbols can be derived from the soft output of the channel decoder to reconstruct the waveform. Soft IC is beyond the scope of this paper and we focus on interference cancellation upon successful decoding which we refer to as post decoding IC.

Post Decoding Interference Cancellation

In this section, we describe in general the basic processing blocks required to support post decoding interference cancellation, as illustrated in Figure 4. We also describe the interaction between H-ARQ operation and IC.

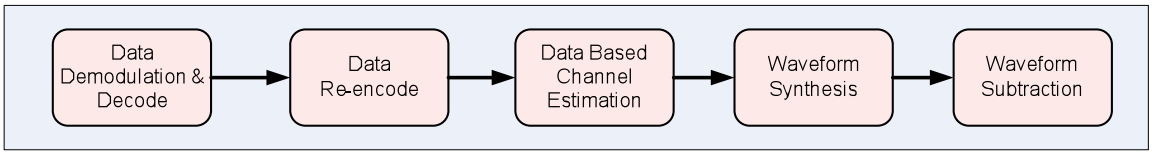

Figure 4: Generic Block Diagram of Data Directed Interference Cancellation

Data Demodulation and Decode

Figure 5 illustrates a block diagram of the Data Demodulation sub-system.

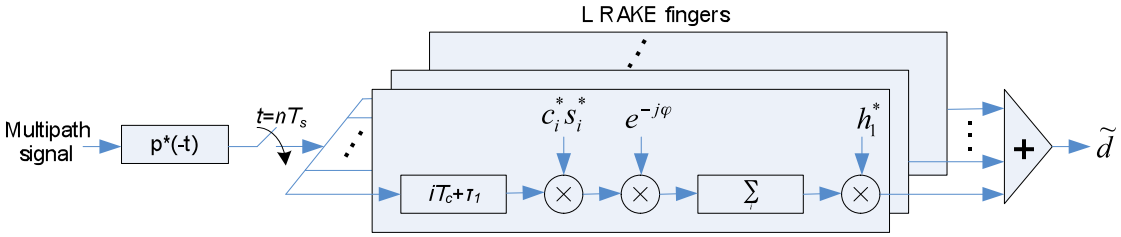

Figure 5: Block diagram of Data Demodulation

In the uplink of a direct sequence code division multiple access (DS-CDMA) system, the continuous time signal transmitted by a desired user is

$$x(t) = \sum_i d_{\lfloor i/N \rfloor} c_i s_i p(t - iT_c),$$

where $d_{\lfloor i/N \rfloor}$ is the data symbol, c_i and s_i are spreading and scrambling code sequences, N is the spreading factor, p(t) is the raised cosine filter, and Tc is the chip duration. The baseband equivalent L-path channel is represented by

$$h(t) = \sum_{l=1}^{L} h_l \delta(t - \tau_l).$$

The received signal after the chip matched filter is

$$r(t) = \sum_{l=1}^{L} \sum_i h_l e^{j\varphi} d_{\lfloor i/N \rfloor} c_i s_i^* q(t - iT_c - \tau_l) + w(t),$$

where $q(t) = p(t) * p^*(-t)$ is the composite response of transmitter and receiver filter, $\varphi = 2\pi\Delta f_i$ is the phase offset due to Doppler frequency, and w(t) is additive Gaussian noise. Without loss of information, the received signal is sampled at twice the chip rate, referred to as chipx2. The discrete samples of the received signal are

$$r[n] = r(t)\big|_{t=\frac{nT_c}{2}} = \sum_{l=1}^{L}\sum_{i} h_l e^{j\varphi} d_{\lfloor i/N \rfloor} c_i s_i q\left(\frac{nT_c}{2} - iT_c - \tau_l\right) + w[n], \quad w[n] \sim CN(0,\sigma^2)$$

where σ^2 is the noise power. The waveform samples are stored in the buffer for further processing. The chipx2 samples are interpolated to recover the path delay. After phase rotation, de-scrambling, and de-spreading, the l-th RAKE finger output for the m-th data symbol is simply

$$\tilde{d}_m^{(l)} = \frac{1}{N}\sum_{i=nN}^{(m+1)N-1} c_i^* s_i^* e^{-j\varphi} r(iT_c + \tau_l) = h_l d_m + w_m^{(l)}, \quad w_m^{(l)} \sim CN(0,\sigma^2/N).$$

With channel estimates, the RAKE receiver performs maximal ratio combining across the outputs of RAKE fingers. The combined symbol is given by

$$\tilde{d}_m = \sum_{l=1}^{L} h_l^* \tilde{d}_m^{(l)} = \sum_{l=1}^{L} |h_l|^2 d_m + w_m, \quad w_m \sim CN\left(0, \sum_{l=1}^{L} |h_l|^2 \sigma^2 / N\right)$$

The combined symbols are sent to the channel decoder. If the transport block is successfully decoded, it will be used to reconstruct the interference for further processing.

Data Re-encode

For the purpose of reconstructing the waveform for cancellation, we need to re-encode the decoded data to recover the chip sequence. Specifically, in our design, the following data channel and overhead channels are re-encoded after successful decoding: DPCCH, DPDCH, PRACH, E-DPDCH, E-DPCCH, HS-DPCCH. In general, the UE's channel coding and multiplexing for these channels are reproduced at the NodeB receiver. The data symbols are spread and scrambled to the chip sequence x_k given as below.

$$x_i = d_{\lfloor i/N \rfloor} c_i s_i .$$

Data Based Channel Estimation

The quality of channel estimation is critical to interference cancellation. If the channel estimate is inaccurate, large residual interference will remain in the signal because the reconstructed signal will not match the true interference. In case of high traffic to pilot power ratios, the decoded data can be used to improve channel estimation performance, which is referred to as data based channel estimation (DBCE). Under the assumption that

the channel is static during M chips, the ML channel estimate is given by the correlation between the data chips and the received signal

$$\hat{h}_l = \frac{1}{ME_c}\sum_{i=0}^{M-1}\left(d_{\lfloor i/N \rfloor}c_i s_i\right)^* r(iT_c + \tau_l) = h_l + z_l, \quad z_l \sim CN(0, \sigma^2/ME_c).$$

It can be seen that DBCE can significantly improve the cancellation efficiency because data chips have higher energy than pilot chips. The correlation length in channel estimation also plays an important role. Smaller estimation variance can be obtained by longer correlation. However, on time-varying channel, estimator may lose coherence if the correlation length is too long. Thus trade-off between variance and coherence must be considered in the design.

Waveform Synthesis

Once the desired user is decoded, its signal could be treated as known interference to other users. Waveform synthesis refers to reconstructing the received waveform samples due to the decoded user via filtering. The reconstructed chipx2 samples will be subtracted from the received sample buffer to cancel the interference. Without loss of generality, we assume channel delays are modeled with resolution of Tc/8, i.e. $\tau_l = \lambda_l T_c / 8$. With knowledge of path delays, phase offsets, and channel estimate, the chipx2 samples to be reconstructed from chip sequence are given by

$$\hat{y}[n] = \sum_{l=1}^{L}\sum_i \hat{h}_l e^{j\varphi} x_i q\left(\frac{nT_c}{2} - iT_c - \frac{\lambda_l T_c}{8}\right).$$

A straightforward method to reconstruct $y[n]$ is called Accumulate/Filter. The re-encoded chip sequence is up-sampled to chipx8 rate. Corresponding to each path, the data chip sequence is weighted by $\hat{h}_l e^{j\varphi}$ and delayed by λ_l samples. Then these paths are accumulated together and passed through the filter $q(t)$. Finally the filter outputs are down-sampled to chipx2 rate. A downside of this method is the filter is working at a chipx8 rate and the implementation requires a true multiplier. This will challenge the hardware design and complexity. An alternative method is called Filter/Accumulate. In this method here the chipx2 samples of each path are reconstructed first. The samples for l-th path is given by

$$\hat{y}^{(l)}[n] = \sum_i x_i \hat{h}_l e^{j\varphi} q\left(\frac{nT_c}{2} - iT_c - \frac{\lambda_l T_c}{8}\right)$$

Among them, the even and odd samples can be written as

$$\hat{y}^{(l)}[2n] = \sum_i x_{n-i}\hat{h}_l e^{j\varphi} q\left(iT_c - \frac{\lambda_l T_c}{8}\right) = \sum_i x_{n-i} q^{even}[i],$$

$$\hat{y}^{(l)}[2n+1] = \sum_i x_{n-i}\hat{h}_l e^{j\varphi} q\left(iT_c - \frac{(\lambda_l - 4)T_c}{8}\right) = \sum_i x_{n-i} q^{odd}[i],$$

The above waveform synthesis procedure is known as poly-phase filtering, in which the convolution on even (odd) stream represents a one-dimensional filter. The index n is in the chip domain and henceforth the filtering happens at the chip rate. The filter coefficients can be updated at a much slower rate (with the same speed of channel estimation). Furthermore, due to the discrete value of data chips, the filter can be

implemented with inverters and adders to avoid true multipliers. Since the waveform synthesis is implemented by filtering the chip sequence, it is also referred to as interference filtering. The filter outputs are multiplied with the channel estimate. Finally multiple paths are accumulated together to reconstruct the composite interference.

$$\hat{y}[2n] = \sum_{l=1}^{L} \hat{y}^{(l)}[2n], \quad \hat{y}[2n+1] = \sum_{l=1}^{L} \hat{y}^{(l)}[2n+1]$$

H-ARQ and Interference Cancellation

H-ARQ operation on the uplink introduces multiple design options with regard to interference cancellation. The cancellation algorithm depends on the depth of the received sample buffer. For example, in Figure 6, if we store a waveform spanning 4 H-ARQ transmissions, and the user decodes on the 4th H-ARQ attempt, then one option is to reconstruct and cancel the waveform corresponding to all H-ARQ attempts after the 4th H-ARQ attempt. This in turn provides benefit to other un-decoded users whose transmissions may have overlapped with this user's previous H-ARQ transmissions. This benefit can be maximized by re-demodulating the previous H-ARQ transmissions for other users prior to their H-ARQ combining and decoding. For example, the cancellation of the User#1's 2nd H-ARQ transmission reduces the interference to User#2's 2nd H-ARQ transmission, as well as User#3's 1st H-ARQ transmission and so on. As another alternative, if we are constrained by the received sample buffer size, a subset of the previous H-ARQ transmissions can be cancelled at the price of a slight degradation in system performance.

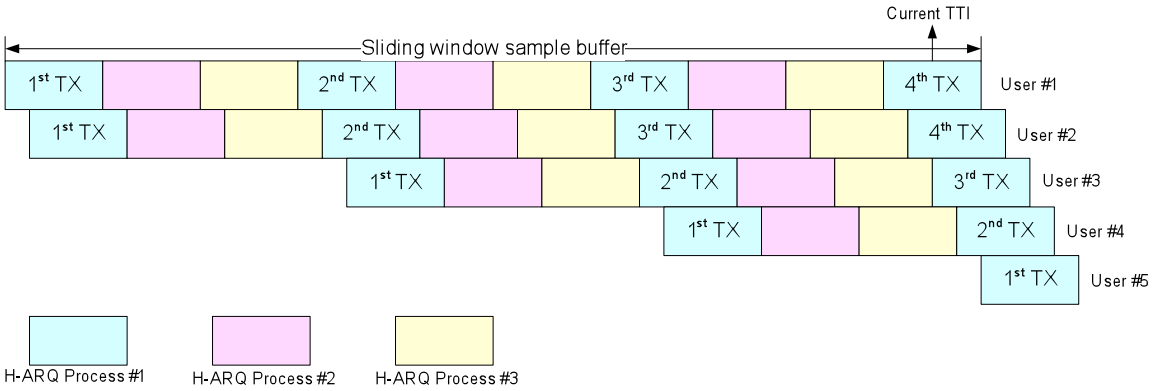

Figure 6: H-ARQ and Interference Cancellation

Implementation of UL Interference Cancellation in HSPA

Uplink Channels in HSPA

Figure 7 illustrates the physical channels on the uplink in WCDMA HSPA. Dedicated channels in the Release 99 specification are employed to transmit circuit-switched voice and data traffic.

- **Dedicated Physical Control Channel (DPCCH):** This channel carries pilot, and control information. The control information includes Transport Format Combination Indicator (TFCI) bits, Transmit Power Control (TPC) bits and Feedback Indicator (FBI) bits.
- **Dedicated Physical Data Channel (DPDCH):** This channel carries dedicated data information. A typical application carried on this channel is AMR 12.2kbps circuit switch voice. The transmission time Interval (TTI) for this channel could be 10ms, 20ms, 40ms, or 80ms.
- **High Speed Dedicated Physical Control Channel (HS-DPCCH)** : This channel carries the feedback from UE about ACK/NACK and CQI information to support the downlink transmissions.
- **E-DCH Dedicated Physical Data Channel (E-DPDCH):** This channel is used to carry uplink data for the E-DCH transport channel. Multi-code and high order modulation scheme are employed to increase the peak data rate. The transmission time Interval (TTI) for this channel could be 2ms or 10ms. Contiguous TTIs are divided into a number of H-ARQ processes (8 processes for 2ms TTI and 4 processes for 10ms TTI). Upon receiving feedback from the NodeB on the decoding result of previous transmission on the H-ARQ process, the UE will transmit a new transport block or retransmit the previous transport block through H-ARQ operation.
- **E-DCH Dedicated Physical Control Channel (E-DPCCH):** This is an uplink physical channel that carries control information associated with E-DPDCH. The information represents the transport format used on the E-DPDCH and the H-ARQ retransmission sequence number.
- **Physical Random Access Channel (PRACH):** This physical channel is used to perform random access on the uplink.

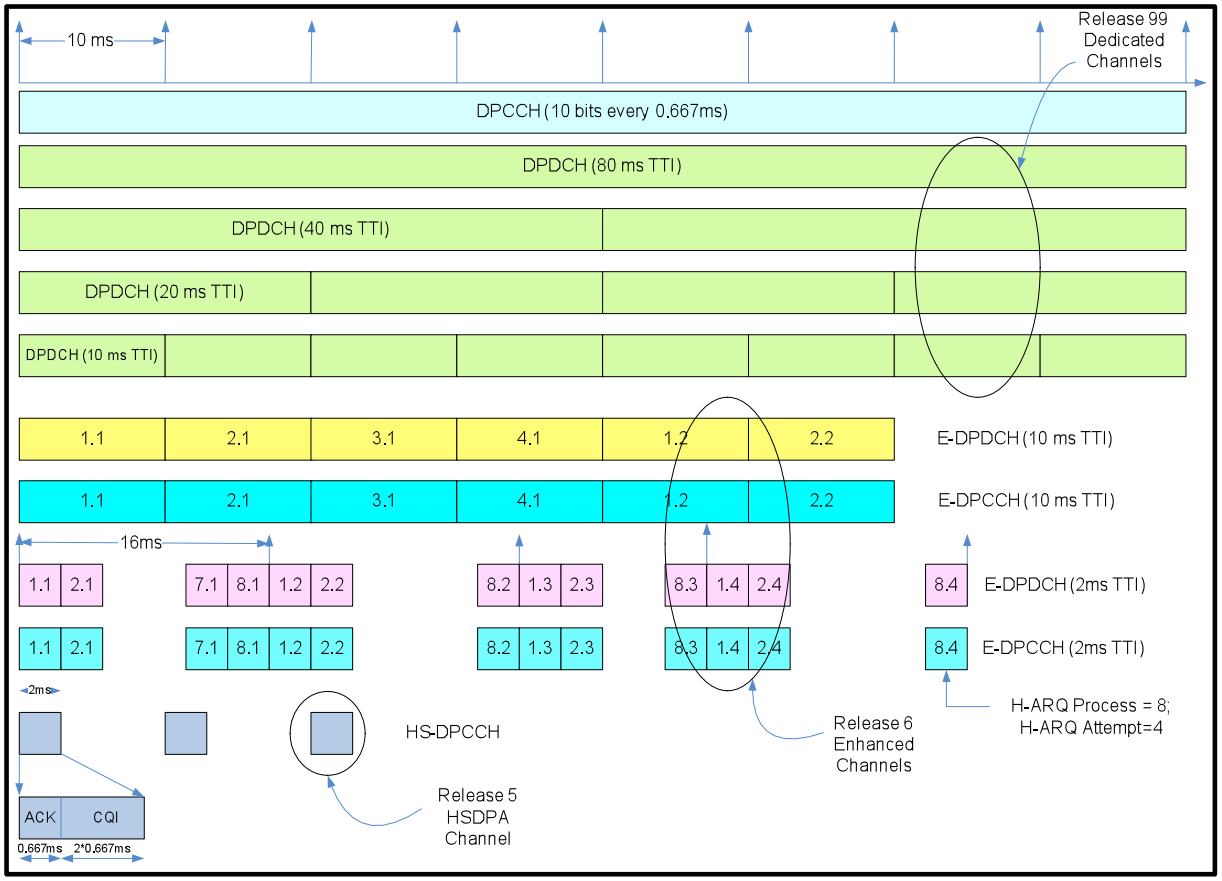

Figure 7: Uplink Channels in HSPA

High Level Block Diagram

Figure 8 illustrates a high level block diagram of the sub-systems corresponding to pilot, overhead and traffic cancellation. As seen in this figure there are three major storage buffers.

- The raw antenna sample input buffer is a real time buffer intended to serve the following sub-systems:
  - Pilot and Overhead demodulation and decode (PODD)
  - Pilot and Overhead interference cancellation (POIC)
- For each user, the pilot demodulator history buffer stores relevant channel estimate information that can be used by the IC sub-systems.
- The modified antenna sample buffer is continuously updated with cancelled waveforms from both the POIC and Traffic interference cancellation (TIC) sub-systems.

These subsystems are described in detail in the following sections.

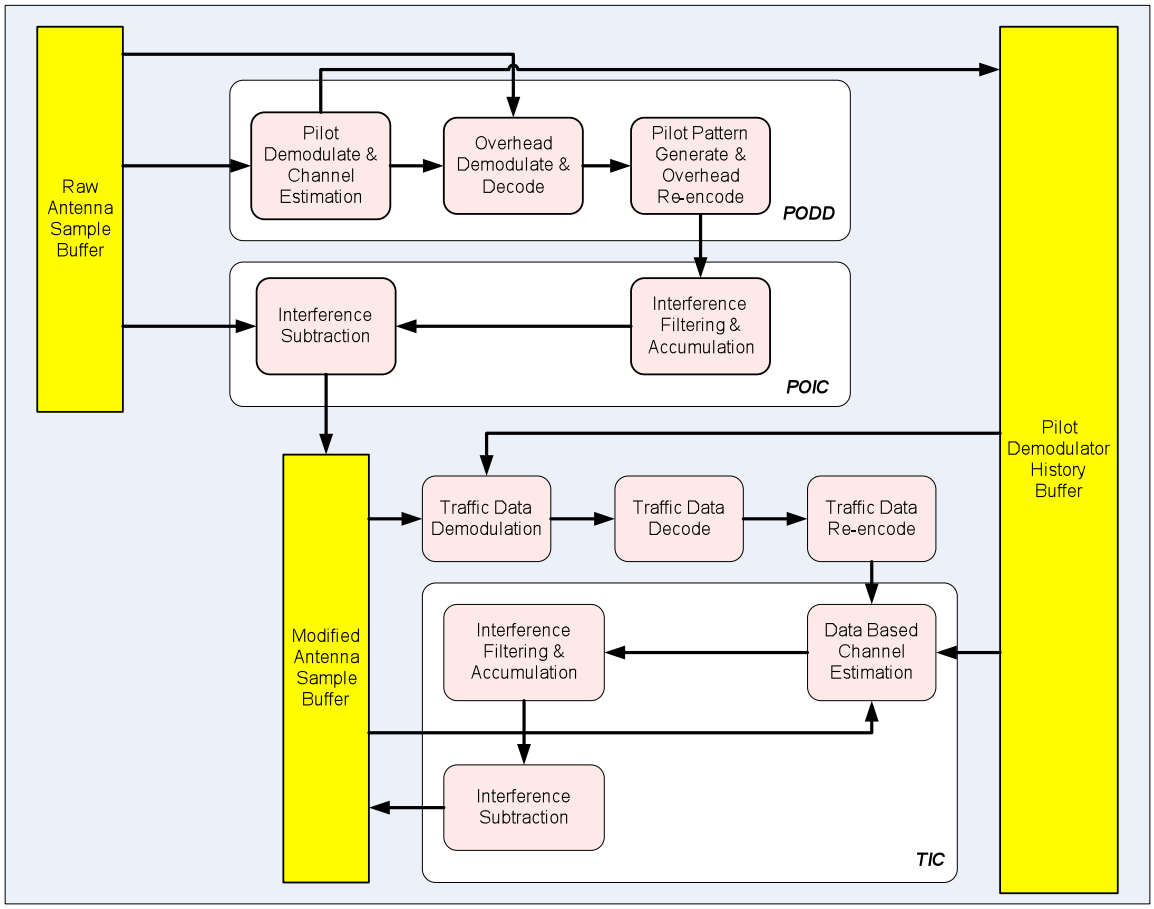

Figure 8: Uplink Interference Cancellation Block Diagram

Pilot and Overhead Demodulation and Decoding

Pilot and overhead demodulation and decoding block processes the following channels: DPCCH, HS-DPCCH and E-DPCCH.

The DPCCH processing block processes basic operations related to DPCCH. The processing includes per-finger processing and combiner processing. Each of the processing includes:

- Per-finger processing
  - DPCCH front-end processing, which includes descrambling, de-spreading, and phase rotation.
  - Pilot filtering for channel estimation.
  - Noise estimation for the purpose of power control and overhead channel detection.
  - Maximal ratio combining (MRC) weight calculation.
  - Finger strength and lock detection.
  - Time tracking loop.
- Combiner Processing

    - Frequency tracking loop
    - Power control.
    - Maximal ratio combining (MRC)

- DPDCH information processing, which includes TPC bits detection and TFCI bits decoding.

The HS-DPCCH sub-block performs HS-DPCCH related processing. The processing includes

- HS-DPCCH front-end processing, which includes descrambling, de-spreading, accumulation, and phase rotation.
- HS-DPCCH symbol combining.
- HS-DPCCH ACK/NACK/DTX detection.
- HS-DPCCH CQI decoding with optional reliability detection.

The E-DPCCH sub-block processes E-DPCCH related operations. The processing includes

- E-DPCCH front-end processing, which includes descrambling, de-spreading, accumulation, and phase rotation.
- E-DPCCH symbol combining
- E-DPCCH DTX detection
- E-DPCCH information decoding with optional reliability detection.

Pilot and Overhead Interference Cancellation

The purpose of the pilot and overhead channel interference cancellation is to generate a replica of the pilot interference signals (DPCCH) and overhead interference signals (HS-DPCCH) accumulated over all fingers and then remove them from the received samples. The implementation of pilot interference cancellation (PIC) and overhead interference cancellation (OIC) are almost identical.

The POIC sub-system consists of the following processing blocks

- Waveform Synthesis or Interference Filtering (IF)

- Interference Subtraction (IS)

The POIC subsystem is illustrated in Figure 8. Note that pilot and overhead channel cancellation are very identical, except for a few differences:

- HS-DPCCH and DPCCH may use different power[3] settings. Hence the channel estimates from DPCCH need to be properly scaled before reconstructing the HS-DPCCH signals.
- DPCCH is always mapped to Q-branch, while HS-DPCCH channel can be mapped to either Q-branch or I-branch, depending on the number of activated DPDCH channels.
- Pilot symbols are known at the receiver, while symbols on HS-DPCCH channel need to be decoded and re-encoded before signal reconstruction.

The pilot and overhead channel interference cancellation obtains the necessary channel estimate information from the PODD such as timing offset, carrier phase, and pilot based channel estimates for each Rake finger.

Because the incoming signal is stored in antenna buffer at twice the chip rate, the pilot signal is reconstructed on even and odd samples separately. As we have discussed in the previous section, filter/accumulate approach is preferred in the current design and the signal from each finger is reconstructed separately and then combined. The even and odd samples of each finger can be expressed as follows:

$$\hat{y}_\ell^{even}(m) = \sum_k d_k \cdot \sum_{i=1}^{SF} c_{k,i} \cdot s_{k,i} \cdot \left[\hat{h}_\ell \cdot e^{j\varphi} \cdot q_\ell^{even}\left(m - k \cdot SF - i\right)\right]^*$$

$$\hat{y}_\ell^{odd}(m) = \sum_k d_k \cdot \sum_{i=1}^{SF} c_{k,i} \cdot s_{k,i} \cdot \left[\hat{h}_\ell \cdot e^{j\varphi} \cdot q_\ell^{odd}\left(m - k \cdot SF - i\right)\right]$$

where k is symbol index, i and m are chip indices. Channelization code and scrambling code are denoted by $c_{k,i}$ and $s_{k,i}$, respectively. Notice that for pilot reconstruction, the pilot symbol d_k is known at receiver. The interference filters $q_\ell^{even}(\cdot)$ and $q_\ell^{odd}(\cdot)$ are specified in the Waveform Synthesis section and are chosen based on the estimate of timing offset τ_ℓ.

Traffic Interference Cancellation (TIC)

The TIC sub-system processes the traffic data channels in HSUPA:

- DPDCH
- E-DPDCH and E-DPCCH
- PRACH that carries the random access messages.

[3] From 3GPP TS 25.213, the allowed gain factors (relative to pilot) for HS-DPCCH are $A_{hs} = \beta_{hs}/\beta c \in [30,24,19,15,12,9,8,6,5]/15$

The traffic demodulation and decoding (TDD) and TIC sub-systems are illustrated in Figure 8. The TDD sub-system reads samples from the Modified Antenna Sample Buffer (MASB). The following functions are executed in the TDD sub-system:

- Timing synchronization
- Descrambling
- De-spreading
- Phase rotation
- MRC combining

In order to benefit from interference cancellation, previous transmissions on the current H-ARQ process are also re-demodulated in TDD. Side information such as timing offset, carrier phase, MRC coefficients, and E-TFC information, are provided by PODD to assist the demodulation and decoding.

The TIC sub-system works on the re-encoded data chips after successful decoding. It mainly consists of three units, data based channel estimation, traffic interference filtering (TIF), and traffic interference subtraction (TIS). The principles under each unit are described thoroughly in previous sections. The design is similar to POIC but implemented in an independent data path. Following interference subtraction, the interference-removed samples are written back to MASB.

The re-demodulation and cancellation of all H-ARQ transmissions requires high processing power of demodulation and cancellation engines. At the same time, the MASB needs a large memory to store the samples across all transmissions. The MASB buffer size can be calculated by the following formula:

$$\text{MASB size} = ((N_{HARQ} - 1) * N_{TX} + 1 + N_{delay}) * f_s * T_{TTI} * W_{sample} * 2$$

N_{HARQ} : the number of H - ARQ processes

N_{TX} : the maximum number H - ARQ transmissions per transport block

f_s : the baseband sampling rate ,

T_{TTI} : the TTI length

W_{sample} : I/Q sample bit width

N_{delay} : Delay allowed by ACK/NACK timeline

For example, for 10ms TTI, 100 slots of samples are required to cancel 2 H-ARQ transmissions. Assuming chipx2 sample rate with 8-bit per sample, the MASB size per antenna is ~1MB. High bandwidth between processing unit and memory may become a design bottleneck. To overcome these design challenges, reduced complexity techniques, such as demodulation and cancellation of a subset of H-ARQ transmissions, can be used to meet the tradeoff between complexity and performance.

TIC Scheduler

A scheduler for dynamic interference cancellation accounts for metrics that could help determine the most likely user to decode amongst a group of users. In this section, we highlight these metrics along with a qualitative discussion of how these metrics could help determine the correct decoding order.

TIC Scheduling Metrics

The role of the TIC scheduler is to dynamically decide an optimal decoding order for a group of users. Below we list some key metrics that may allow the TIC scheduler to prioritize users who are most likely to decode:

- **H-ARQ Attempt Number:** A user on the 4^{th} attempt is more likely to decode than on the 1^{st} attempt. As a result, there is an advantage in trying to decode the 4^{th} attempt user v/s the first attempt user.
- **Payload Size:** It maybe useful to decode a user with a higher payload size (and hence a higher T/P) compared to a user with a lower payload size, because if this user decodes, we would have removed more interference for other users.
- **IC Iteration Number/ Amount of energy removed since the last decode attempt:** At any given time during scheduling, we may want to give higher priority to a user who failed to decode in the first iteration but there was sufficient energy removed from his waveform since the previous iteration attempt.
- **ACK Response Time Deadline:** The timing requirement for the ACK/NACK response to an uplink E-DPDCH channel on the downlink E-HICH channel is 6.4 ms for the 2ms TTI and 14.4 ms for the 10ms TTI. This timing requirement serves as an important input to the TIC scheduler. If close to the ACK response deadline, and have yet to demodulate and decode a user even once, the scheduler may need to place this user at the head of the queue.
- **Pilot Strength:** A user's pilot strength (i.e. Ecp/Nt) could solely decide if we should attempt to decode this user. A stronger pilot leads to superior channel estimation and hence a better chance of demodulation and decoding.
- **Number of Fingers required:** Generally, a packet with larger number of independent paths will provide more frequency diversity, but also requires more hardware (finger) resources to be processed. Therefore, a packet with larger number of paths may get higher priority if the TIC scheduler wishes to process the more likely-to-decode packet first, or may get lower priority if hardware resource is limited and low processing delay is the target.
- **Eb/Nt:** This metric takes into account H-ARQ attempt number, Ecp/Nt as well as T/P ratio and can be used to index into an appropriate BLER curve.
- **QOS Setting**: A user's QOS setting may dictate the order in which a user may be demodulated and decoded.

TIC Processing Pipeline

Baring in mind the pipeline structure and processing delay of hardware implementation, the whole IC processing can be illustrated as a timeline, see Figure 9. The figure is illustrative of the TIC operation. In particular we focus on the cancellation of E-DCH transmissions.

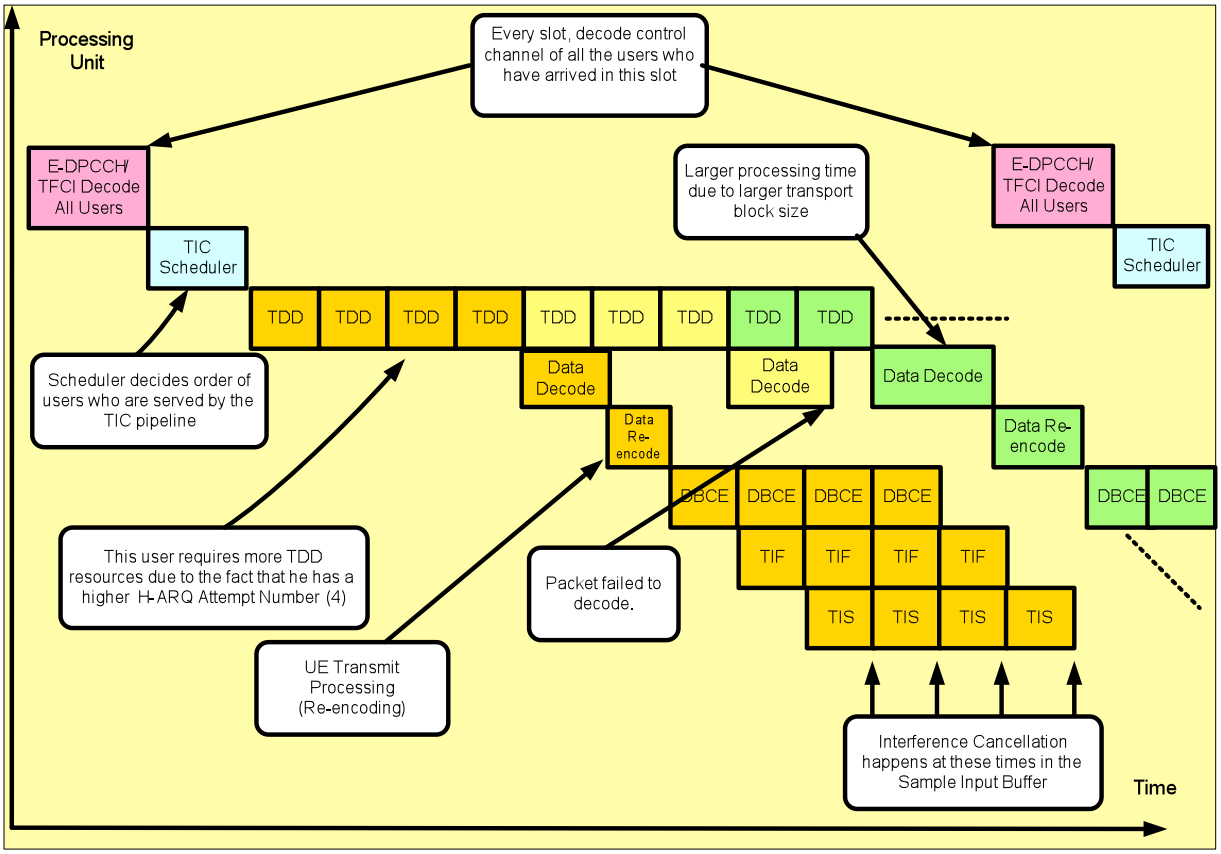

Figure 9: Uplink Interference Cancellation Processing Timeline

When a packet arrives at the antenna input, it is processed by different stages of the IC sub-system until the deadline to respond with an ACK/NACK to the UE. Every slot, the TIC scheduler dispatches packets to the TIC processing pipeline. Packets are dispatched to the TDD, Data Decoder, DBCE, TIF and TIS in a sequential manner. Due to the delay of the pipeline, the packets dispatched before the time instant when a packet was cancelled will not benefit from the cancellation of this packet. These packets will still benefit from packets that were already cancelled from the MASB prior to their dispatch time. Note that if a packet fails to decode and there is still time to respond with an ACK/NACK back to the UE, the TIC scheduler may chose to re-dispatch this packet to the pipeline. This technique can be deemed as a form of iterative group IC where a group corresponds to a set of users that operate in parallel on the same waveform.

UL IC Performance Study

IC Efficiency Performance

In this section, we present the link-level performance of interference cancellation in HSUPA by investigating the IC efficiency as a function of instantaneous Signal to Noise Ratio (SNR). We have stressed that the channel estimation quality is critical to cancellation efficiency. The principle of data-based channel estimation was presented earlier. For 2ms TTI, data-based channel estimation is done by one-slot averaging due to the short length. For 10ms TTI, data-based channel estimation is obtained by 4-slot non-causal averaging.

The cancellation efficiencies vs Ec/Nt are shown in Figure 10 and Figure 11. Several typical channel models in 3GPP, Ped A 3km/h, Ped B 3km/h, Veh A 30km/h, Veh B 120km/h, and Typical Urban 3km/h, are used to evaluate the cancellation efficiency.

From the simulation results, we observe in general

- Cancellation efficiency increases as the data channel SINR;
- Slow fading channels have better cancellation efficiency than more dynamic channels;
- Cancellation efficiency of 10ms TTI is higher than 2ms TTI due to better channel estimation.

Under close loop power control, the nominal range of pilot channel SINR is -25dB~-20 dB for HSUPA operation; the data channel SINR is in the range of -20dB~-5dB. As seen from these simulation results, cancellation efficiency of more than 70% can be expected for the data channel.

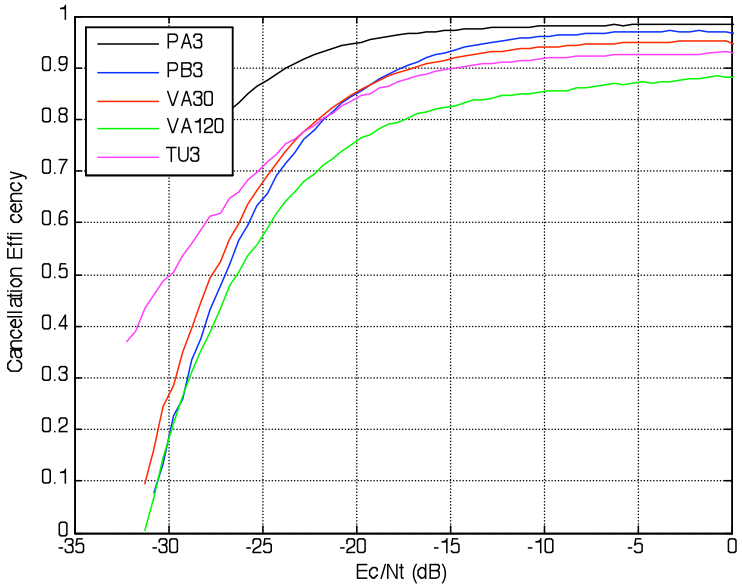

Figure 10: Interference Cancellation Efficiency of 2ms TTI

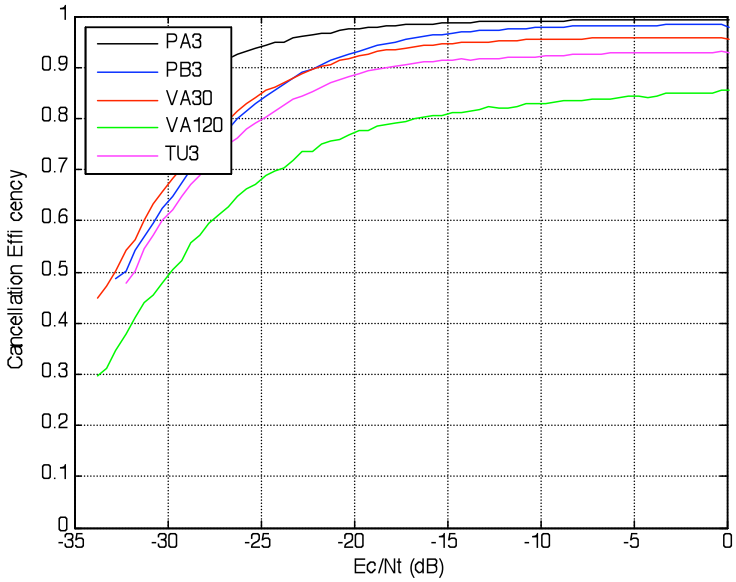

Figure 11: Interference Cancellation Efficiency of 10ms TTI

System Performance

In this section, we provide the system-level simulation results for the gains of interference cancellation. The simulations are based on the standard 3GPP evaluation methodology [7]. A network of 19 NodeBs with 3 cells per NodeB is implemented with MAC and Physical layers according to the HSUPA standard. A full buffer traffic model is employed to study the system capacity. The simulation assumptions are listed in Table 1.

Table 1: System Simulation Assumptions

Parameter	Value	Comments
Network Layout	19 NodeBs	Wrap-around topology
Site-to-site Distance	2.8km	
Cells per NodeB	3	
Receive Antennas per Cell	2	
UE Max Power	21dBm	
Channel Types	3GPP Mix	Ped A 3km/h = 30% Ped B 3km/h = 30% Veh A 30km/h = 20% Veh A 120km/h = 20%
UE Active Set Size	≤3	
E-DPDCH TTI	2ms	
UEs per Cell	10	Full Buffer Traffic
E-AGCH channels per Cell	2	
Scheduling Algorithm	Proportional Fair	

Fast NodeB scheduling is one of most prominent features to determine the HSUPA performance. A detailed study of HSUPA scheduling algorithm utilizing interference cancellation can be found in [6]. A similar proportional fair scheduling algorithm is considered here. The users are ordered by the following metric:

$$\text{Priority} = \frac{r_{\text{support}}[k]}{T[k]},$$

where $r_{\text{support}}[k]$ is the maximal supported rate by the UE as allowed by it's transmit power headroom, and $T[k]$ is the long-term average throughput of the UE at time k. In the presence of interference cancellation, the effective noise rise seen by the decoder after interference cancellation is controlled by the NodeB scheduler to meet the network stability criterion. The effective noise rise is measured in a time window of 15 slots with a 7-slot delay. Under a target effective noise rise constraint, the available load is allocated to the UEs by their priorities.

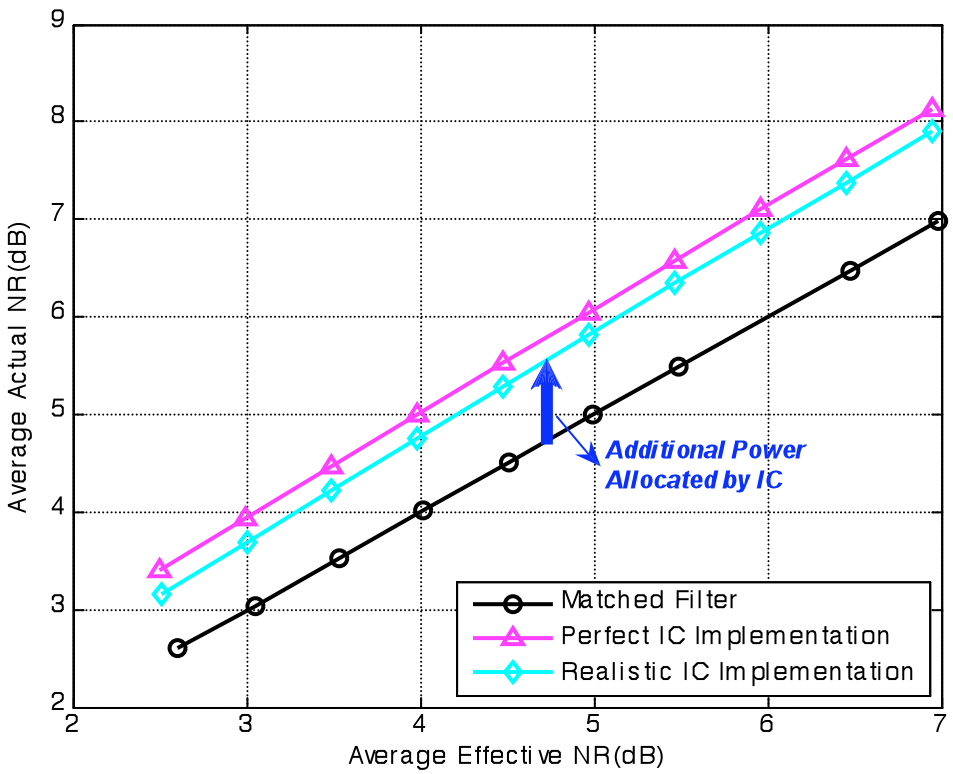

Figure 12: Actual Noise Rise v/s Effective Noise Rise: 2Rx Antennas, 10 UEs per cell

Figure 12 compares the actual noise rise between IC and non-IC (Matched Filter). Targeting the same effective noise rise, a higher actual noise rise is observed with IC. At 4.5dB effective noise rise, the actual noise rise of IC is close to 5.3dB. The practical IC scheme approaches perfect cancellation. In other words, more interference power is allowed while maintaining the system noise rise stability. The increased noise rise will directly translate to system capacity advantage with IC.

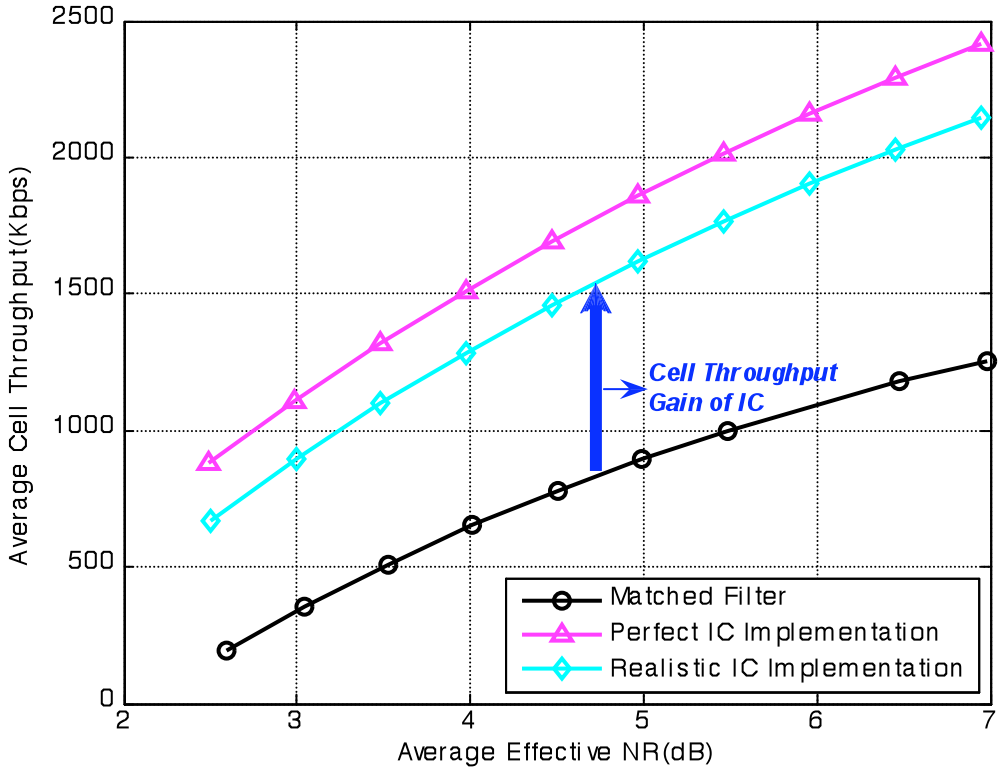

Figure 13: Average Cell Throughput: 2Rx Antennas, 10 UEs per cell

Figure 13 shows the average cell throughput vs effective noise rise. At 4.5dB effective noise rise, the IC schemes can achieve a cell throughput of 1460 kbps while 800 kbps is achieved for Non-IC. Observe that a cell throughput gain of greater than 60% is obtained with IC over a wide range of average effective noise rise.

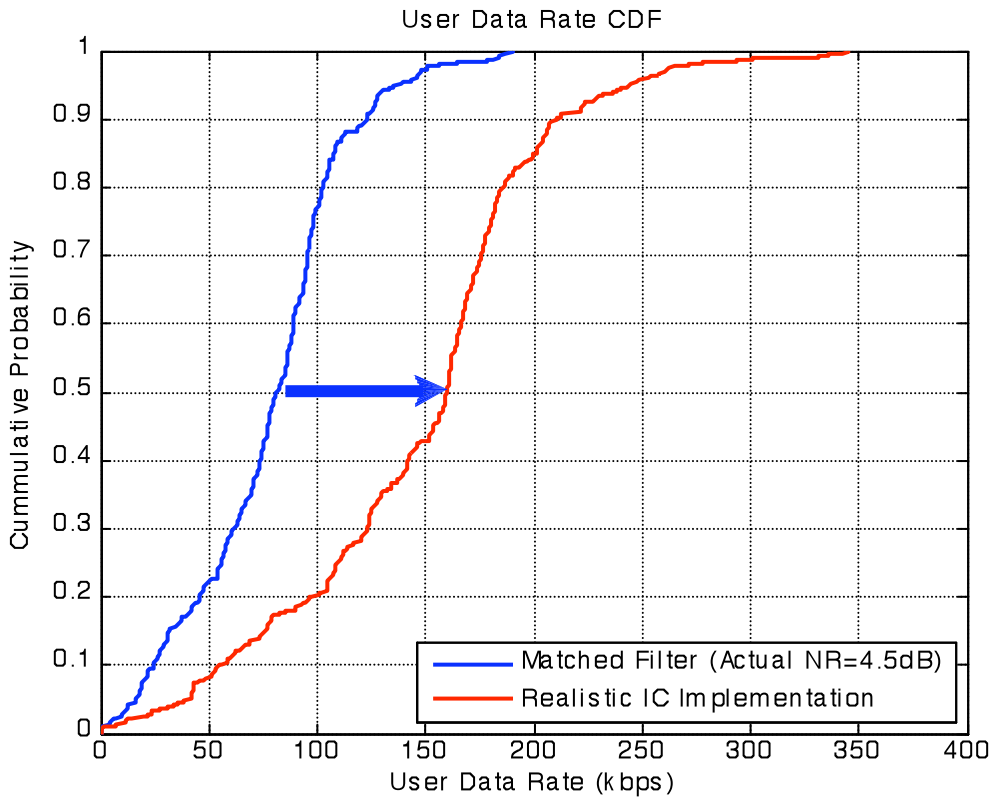

Figure 14: User Data Rate Cumulative Distribution: 2Rx Antennas, 10 UEs per cell

In Figure 14 the cumulative distribution of the user data rate is plotted. Note that with IC, there is a significant shift to higher data rates. The median data rate increases from 80kbps to 160kbps. In addition to cell throughput improvement, this illustrates user experience improvement under IC.

Conclusion

In this paper we have demonstrated the feasibility of uplink IC in W-CDMA/HSPA NodeB receivers. We described the principles of a robust and efficient post decoding IC scheme. The implementation of the proposed scheme in Node B receiver is illustrated in detail. We have shown that the practical uplink IC scheme proposed in this paper significantly enhances system capacity as well as user throughputs throughout the cell. Uplink IC does not require changes to the existing 3GPP specifications and UE modifications. This enhancement is critical to ensuring that HSPA continues to remain a dominant and competitive technology in the evolution of mobile communications.

Acknowledgements

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